REMARKS

Reconsideration of the application is requested.

Claims 1-38 remain in the application. Claims 39-76 are withdrawn from examination.

In item 2 on page 2 of the above-identified Office action, the Examiner requested a restriction to one of the inventions of group I, claims 1-38, or group 2, claims 39-76, under 35 U.S.C. § 121.

A provisional election of group I, claims 1-38 was made on October 3, 2003. Applicants affirm the election to prosecute group I, claims 1-38 with traverse.

In item 8 on page 4 of the above-identified Office Action, claims 1-38 have been rejected as being fully anticipated by Kau et al. (U.S. Patent No. 6,421,754) under 35 U.S.C. § 102.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*:

> A program-controlled unit, comprising:
> an intelligent core configured to process instructions to be executed;
> . . .
> **a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units**, including an interface connection between said intelligent core and said internal peripheral units, between said intelligent core and said external peripheral units, between said intelligent core and said memory devices, and between said plurality of units . . .

In the present invention, the structurable hardware unit 12 (SLE layer) is arranged, in circuit terms, between the µP core 11, peripheral units (for example the peripheral units 13 to 19) provided inside and/or outside the program-controlled unit, and/or memory devices (for example the RAM 2 and/or the ROM 3) (see Fig. 1). It contains **structurable** data paths and/or logic elements which can be structured or configured in such a way that the structurable hardware unit 12 can be used as a **configurable** intelligent interface between the µP core and one or more peripheral units and/or between the µP core and one or more memory devices and/or between two or more peripheral units themselves and/or between one or more peripheral units and one or more memory devices (page 11, lines 9-21 of the instant application).

The structurable hardware unit 12, shown in Fig. 2, has a logic block unit 122, which is the actual core of the unit 12. Logic block unit 122 is extremely flexible. Virtually **any** desired linkages, processing and evaluations of the input signals can be carried out by such universally usable structurable logic arrangements (page 16, line 19 through page 17, line 2). Logic block 122 is divided into sub-blocks. The sub-blocks are configurable multiplexers (**for switching data paths** as desired), registers (for buffer-storing data and/or coded states) and structurable logic (for linking data and/or signals with one another and with constants and for coding and decoding states) (pages 17 and 18 of the instant specification).

Because within the SLE layer 12, there are both direct connections and configurable data paths and data path linkages between the devices which are connected or can be connected via the SLE layer, if the structurable hardware unit 12 has access to memory devices (for example to the RAM 2 and/or to the ROM 3) it can transfer data from and to the memory devices **independently**, i.e. **without the participation of the µP core**, for itself and/or the µP core and/or the peripheral units. As a result, data transfers can be carried out more rapidly and without burdening the µP core 11. In

this case, the structurable hardware unit 12 is constructed in such a way that it can identify and handle contending accesses to memory devices.

The Kau et al. reference discloses a computer docking station (Fig. 1), that allows a computer to easily be connected to a variety of peripheral devices (Fig. 3 and col. 9, lines 2-63). As explained in col. 10, lines 41-52, the docking station provides A) advantageous system expandability through i) ISA/EISA slots, ii) additional HDD space, CDROM, multimedia with monaural, stereo, quadraphonic and other sound systems, and iii) wide bandwidth PCI bus 71 local bus slots. A further area of advantage B) is quick, easy connections to desired non-portable equipment through i) easier to use, bigger keyboard, ii) bigger, higher quality, CRT display iii) better mouse, printer, and so on. For example, the user merely pushes the notebook 6 into the docking station 7 quickly and easily, and all peripherals are then hooked up, without any further user hookup activity.

As shown in Fig. 3 of Kau et al., bus 104 connects microprocessor unit (MPU) 102 with the above-mentioned peripheral devices. A block diagram of MPU 102 is shown in Fig. 9. A DOS-compatible static 486 core in MPU 102 allows on-the-fly clock-scale and clock-stop operation to conserve

battery power (col. 12, lines 58-66). The MPU 102 is suitably a static device wherein no internal data is lost when the clock input is stopped or clock-modulated by turning the clock off and on repeatedly (col. 13, line 66 through col. 14, line 2).

As is explained in col. 13, lines 59-66, power management block 708 provides a dramatic reduction in current consumption when the microprocessor MPU 102 is in standby mode. Low voltage operation, such as 3.3 volts or less, coupled with power management, provides the capability to achieve low system battery power consumption (col. 12, lines 58-66). Standby mode is entered either by a hardware action in unit 920 of PPU 110 or by a software initiated action. Standby mode allows for CPU clock modulation, thus reducing power consumption. MPU power consumption can be further reduced by generating suspend mode and stopping the external clock input.

More specifically, as recited in col. 14, lines 7-22 of Kau et al., core 702 simply has a system-management mode with an additional interrupt and a **separate address space** that is suitably used for **system power management or software transparent emulation of I/O (input/output) peripherals.** The system management mode is entered using a system management

interrupt, which has a higher priority than any other interrupt and is maskable. While running in the **separate address space**, the system management interrupt routine advantageously executes without interfering with the operating system or application programs. After reception of the system management interrupt, portions of the CPU are automatically saved, system management mode is entered and **program execution begins in the separate address space.** (col. 14, lines 7-22).

Kau et al. simply provides a software controlled power management circuit configuration that adjusts the speed of the core of a microprocessor unit. Kau et al. do not have an SLE layer 12, as does the present invention. In Kau et al., the peripheral devices are connected directly to MPU 102 via main bus 71, interconnected to bus 104 (col. 8, line 66 through col. 9, line 2). In contrast, the SLE layer 12 of the present invention has structurable data paths and/or logic elements which can be structured or configured in such a way that the SLE layer 12 can be used as a configurable intelligent interface between the μP core and one or more peripheral units and/or between the μP core and one or more memory devices and/or between two or more peripheral units themselves and/or between one or more peripheral units and

one or more memory devices (page 11, lines 13-21 of the instant application).

Clearly, Kau et al. do not show a structurable **hardware unit** selectively forming an application-specifically **configurable** intelligent **interface for respectively connecting an intelligent core and the units**, as recited in claim 1 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-38 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required for this paper, Petition is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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